U.S. Patent No. 5,652,450 to Hirano. The rejection is respectfully traversed.

Applicant has amended claim 1 for clarity to insert the word "gate" to recite the presence of a "split-gate" structure. Applicant respectfully submits that the Examiner has cited no portion of Hirano suggesting the structure of claim 1 including a "split-gate" structure. Accordingly, the rejection should be withdrawn. Dependent claims 2-5, 7, 9, 23 and independent claim 32 can be distinguished in a manner similar to claim 1. Applicant also notes that claims 4 and 9 were amended for clarity.

Claim 8 was rejected under 35 U.S.C. 103(a) as unpatentable over Hirano. The rejection is respectfully traversed. Claim 8 depends from claim 1 and can be distinguished in a manner similar to claim 1. In addition, applicant notes that the Examiner stated at pages 5 and 6 of the Office Action that "Although Hirano's device does not teach the exact impurity concentrations as claimed by Applicant, the concentration differences are considered obvious . . ." However, the portions of Hirano cited by the Examiner do not appear to describe or suggest any particular impurity concentrations. Accordingly, applicant respectfully submits that the Examiner has provided an improper basis for the rejection and the rejection should be withdrawn.

Claim 31 was rejected over Hirano in view of U.S. Patent No. 6,242,773 to Thomas. The rejection is respectfully traversed. Applicant respectfully submits that the Examiner has cited no portion of the art that describes or suggests a "non-volatile memory transistor having a split gate structure" as recited in claim 31. Accordingly, the rejection should be withdrawn.

Claims 10-11, 16-20, 25 and 28-30 were rejected under 35 U.S.C. 103(a) as unpatentable over Hirano in view of U.S. Patent No. 5,654,577 to Nakamura and U.S. Patent No. 5,650,344 to Ito et al. The rejection is respectfully traversed.

To establish a prima facie case of obviousness, the following criteria should be met. First, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings. Second, there should be a reasonable expectation of success. Third, the reference(s) must teach all the claim limitations. MPEP section 706.02(j). Applicant respectfully submits that the Examiner's citations to the art are insufficient to satisfy the three criteria above and accordingly, the rejection should be withdrawn.

The Examiner cited no portion of the art that describes or suggests motivation for or the desirability of the combination of Hirano and Nakamura. In addition, the Examiner did not

provide any basis for a reasonable expectation of success in making the proposed combination. In addition, these claims all depend from claim 1, which has been discussed above. Applicant respectfully submits that the Examiner has cited no portion of the art the describes or suggests a "split-gate" structure as recited in claim 1. As described above, the three criteria for establishing obviousness have not been met and the rejection should be withdrawn. Applicant also notes that claim 25 was amended for clarity. Claims 10-11, 16-20, 25 and 28-30 can be similarly distinguished.

Claims 12-15, 21 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Nakamura and further in view of U.S. Patent No. 6,242,773 to Thomas. The rejection is respectfully traversed. The Examiner cited no portion of Nakamura and Thomas that overcomes the deficiencies of Hirano as discussed above for claim 1 (from which claims 12-15, 21 and 22 depend). Accordingly, these claims can be distinguished over the cited art for the same reasons as claim 1. In addition, claim 15, which was amended as described earlier, recites in part that the "insulation layer between the first and second outermost layers that is formed by a CVD method is a silicon oxide layer." Applicant respectfully submits that the Examiner has cited no portion of the art the suggests such an insulation layer. For example, it appears that the Examiner's citation to an ONO layer in Thomas refers to a silicon nitride layer 120 between layers 118 and 124. Accordingly, claim 15 is also patentable over the cited art for this reason.

Claim 22, which was also amended as described earlier, recites in part "the layer formed between the first and the second outermost layers comprises a silicon oxide layer." Claim 22 can be distinguished over the cited art in a similar manner as claim 15.

Claims 6 and 24 were objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form. Applicant has rewritten claims 6 and 24 in independent form. Applicant notes that for claim 6, language from original claim 2, which was in the chain of claims from which claim 6 depended, was amended to delete "selected from the group consisting of positive and negative voltages" and insert "including positive and negative voltages" in its place.

Applicant has added new dependent claims 33-34. Support for these claims may be found throughout the specification and in the original claims. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-34 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Dated: March 25, 2002

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 25, 2002.

Alan S. Raynes — **March 25, 2002**

Alan S. Raynes — **(Date)**

Version With Markings to Show Changes Made

Claims 1, 4, 6, 9, 15, 22, and 24-27 were amended as follows:

1. (amended) A semiconductor device having a non-volatile memory transistor having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region; and

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well.

4. (amended) A semiconductor device having a non-volatile memory transistor according to claim 2, wherein the semiconductor substrate is a p-type, the first well is an n-type, the second well is a p-type, and each of the [pair of] source and drain is an n-type.

6. (amended) A semiconductor device having a non-volatile memory transistor [according to claim 5, wherein] having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region; and

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor is operated using voltages including positive and negative voltages;

wherein, for writing data in the non-volatile memory transistor, a voltage in an opposite polarity is applied to the control gate, a voltage in one polarity is applied to one of the source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for erasing data in the non-volatile memory transistor, a voltage in the one polarity is applied to the control gate, a voltage in the opposite polarity is applied to one of the

source and the drain, a voltage in the opposite polarity is applied to the other of the source and the drain, a voltage in the opposite polarity is applied to the second well, and a voltage in the one polarity is applied to the first well;

wherein, for writing data in the non-volatile memory transistor, a voltage of –3 V through –4 V is applied to the control gate, a voltage of +3 V through +4 V is applied to one of the source and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well, and

wherein, for erasing data in the non-volatile memory transistor, a voltage of +6 V through +7 V is applied to the control gate, a voltage of –5 V through –6 V is applied to one of the source and the drain, a voltage of –5 V through –6 V is applied to the other of the source and the drain, a voltage of –5 V through –6 V is applied to the second well, and a voltage of +0.9 V through +3.3 V is applied to the first well.

9. (amended) A semiconductor device having a non-volatile memory transistor according to claim 1, wherein the non-volatile memory transistor has a [first] gate insulation layer, [a second gate insulation layer,] a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer, wherein

the [first] gate insulation layer [and the second gate insulation layer are] is located above the second well and between one of the [pair of] source and drain and the other of the [pair of] source and drain,

the floating gate is located above the first gate insulation layer,

the intermediate insulation layer is located above the floating gate and the semiconductor substrate, and

the control gate is located above the [second gate] intermediate insulation layer and rests on the floating gate through the intermediate insulation layer.

15. (amended) A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the insulation layer between the first and second outermost layers that is formed by a CVD method is a silicon oxide layer [is] formed by [the] a CVD method selected from a group consisting of a HTO (high temperature oxide) method and a TEOS (tetraethyl orthosilicate) method.

22. (amended) A semiconductor device having a non-volatile memory transistor according to claim 14, wherein the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor has a film thickness of 5 – 15 nm, and the second outermost layer has a film thickness of 1 – 10 nm, and the [silicon oxide] layer formed between the first and the second outermost layers comprises a silicon oxide layer having [has] a film thickness of 10 – 20 nm.

24. (amended) A semiconductor device having a non-volatile memory transistor [according to claim 10, wherein the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V, the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and the third voltage level that operates the third voltage-type transistor is 10 – 15 V] having a split-gate structure, the semiconductor device comprising:

a semiconductor substrate of a first conductivity type having a memory region;

a first well of a second conductivity type located in the memory region;

a second well of a first conductivity type located in the first well, wherein the non-volatile memory transistor includes a source and drain that are located in the second well;

wherein the non-volatile memory transistor has a first gate insulation layer, a second gate insulation layer, a floating gate, a control gate and an intermediate insulation layer functioning as a tunnel insulation layer,

wherein the first gate insulation layer and the second gate insulation layer are located above the second well and between one of the pair of source and drain and the other of the pair of source and drain, the floating gate is located above the first gate insulation layer, the intermediate insulation layer is located above the floating gate, and the control gate is located above the

second gate insulation layer and rests on the floating gate through the intermediate insulation layer;

wherein the semiconductor substrate includes first, second and third transistor regions including field effect transistors that operate at different voltage levels, wherein the first transistor region includes a first voltage-type transistor that operates at a first voltage level of 1.8 - 3.3 V, the second transistor region includes a second voltage-type transistor that operates at a second voltage level of 2.5 - 5 V, and the third transistor region includes a third voltage-type transistor that operates at a third voltage level of 10 - 15 V, and

wherein the second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

25. (amended) A semiconductor device having a non-volatile memory transistor according to claim 10, further comprising at least a flash-memory (flash EEPROM), wherein the flash-memory includes a memory cell array [composed of] comprising non-volatile memory transistors and peripheral circuits formed therein.

26. (amended) A semiconductor device having a non-volatile memory transistor according to claim 25, further comprising another circuit region mixed together with the flash-memory (flash EEPROM) on the substrate.

27. (amended) A semiconductor device having a non-volatile memory transistor according to claim 26, wherein the circuit region includes at least [a] a logic circuit.